

**REMARKS**

Claims 1, 3-9, 11-16, 22, 23, 25, 27-29, 31-33, 35-36, 41, 43-45, 47-49, 50, and 51 are pending in this application. Claims 1-52 stand rejected. By this Amendment, claims 1, 3, 4, 9, 11, 12, 29, 31, 32, 41, 43, and 44 have been amended and claims 2, 10, 17-21, 24, 26, 30, 34, 37-40, 42, 46, and 50 are canceled without prejudice. The amendments to the claims have been made to improve the form thereof. In light of the amendments and remarks set forth below, Applicants respectfully submit that each of the pending claims is in immediate condition for allowance.

Claims 1-16, 25-44, and 49-52 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,952,948 ("Proebsting") in view of U.S. Patent No. 6,201,523 ("Akiyama"). Applicants respectfully traverse this rejection.

Among the limitations of Applicants' claims not present in the cited references is a sampling circuit that comprises a plurality of pairs of switches and a pair of switches is simultaneously activated and have an approximate same resistance value when the pair of switches is activated.

Each of independent claims 1, 3, 4, 9, 11, and 12 explicitly recite that the sampling circuit comprises a plurality of pairs of switches and a pair of switches is simultaneously activated and have an approximate same resistance value when the pair of switches is activated. Proebsting fails to disclose this explicitly recited limitation nor does Akiyama.

The Office Action asserts that this feature is disclosed in Figure 4 as items 404, 406, 408 and in column 4 lines, 26-30. Applicants respectfully traverse this rejection. Applicants have amended the independent claims to recite that the sampling circuit comprises a plurality of pairs of switches, a pair of switches being simultaneously activated and each has an approximate same resistance value when the pair of

switches is activated. This feature is not disclosed in Proebsting. In Proebsting, switches 404 and 406 merely act as resistor elements that form part of the overall voltage divider chain. However, there is no disclosure of the approximate same resistance as explicitly recited in Applicants' claim. Therefore, Applicants respectfully submit that all of their independent claims are allowable over the cited references.

Additionally, Applicants note that the explicitly claimed configuration whereby a pair of switches is simultaneously activated. In accordance with the claimed invention, a driving circuit comprises a digital-to-analog conversion circuit and a sampling circuit and/or a variable resistance circuit. The driving circuit according to the claimed invention discloses that a plurality of voltages V0-V4 supplied from an external source is divided to thereby generate the larger number of grayscale voltages than the number of supplied voltages, and the grayscale voltage is distributed to a plurality of signal lines.

Proebsting (USP 5,952,948) discloses a digital-to-analog conversion circuit which generates a lot of grayscale voltages by dividing voltages.

Akiyama(USP 6,201,523) discloses a sampling circuit for distributing grayscale voltage into a plurality of signal lines.

The digital-to-analog circuit of Proebsting merely discloses that a voltage is divided by only resistances included in the digital-to-analog conversion circuit. On the other hand, the driving circuit of the claimed invention discloses that a voltage is divided by a serial resistance of a sampling circuit and a digital-to-analog conversion circuit or by a serial resistance of a sampling circuit and a variable resistance circuit.

Thus, a higher resistance value is obtained compared to the case where a voltage is divided by only a digital-to-analog conversion circuit or by only a variable

resistance circuit. Increasing a resistance for dividing voltage is decreases through-current flowing in the resistance to thereby decrease power consumption.

For example, in Fig. 2, two serial resistances comprise the following elements:

(i) Serial resistance 1: one of a pair of thin film transistors 29 and a thin film transistor 26; and

(ii) Serial transistor 2: the other one of the pair of thin film transistors 29 and a thin film transistor 27.

Fig. 4 shows that a voltage is divided by the resistance ratio of the above serial resistances 1, 2. Fig. 4 shows that a resistance value of each of thin film transistors 26, 27 is any value of  $R_1$  to  $R_3$  and a resistance value of thin film transistor 29 is  $RSW$ . Further, the pair of thin film transistors 29 (included in the sampling circuit) simultaneously is activated to generate a voltage divided by using serial resistances 1, 2. Thereby, the claimed invention discloses that a gate electrode of the pair of thin film transistors is common and the pair thin film transistors receives same control signal from a control circuit 28.

Akiyama merely discloses a configuration in which either one of two signals is alternatively selected. However, Akiyama does not disclose a configuration in which a pair of switches is simultaneously activated. Further, as disclosed in Figs. 2, 7, 10, 13, 16, and 17, and their accompanying disclosure, the features in Applicants' claims. It should be noted that the disclosed configurations achieve a positive and a negative side for a plurality of voltage resources to generate an AC voltage for driving a liquid crystal display. Therefore, the drive circuit configuration of the claimed invention is unlike the prior art.

Applicants have responded to all of the rejections and objections recited in the Office Action. Reconsideration and a Notice of Allowance for all of the pending claims are therefore respectfully requested.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

If the Examiner believes an interview would be of assistance, the Examiner is welcome to contact the undersigned at the number listed below.

Dated: March 6, 2006

Respectfully submitted,

By 

Ian R. Blum

Registration No.: 42,336

DICKSTEIN SHAPIRO MORIN & OSHINSKY  
LLP

1177 Avenue of the Americas  
New York, New York 10036-2714  
(212) 835-1400  
Attorney for Applicants

IRB/mgs

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as Express Mail, Airbill No. EV 451112231 US, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date shown below.

Dated: March 6, 2006

Signature:  (Ian R. Blum)